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Giovanni Agosta
CURRICULUM VITAE

Personal Information

Surname	Agosta
Name	Giovanni
Birth Date	28/XII/1975

Current position

I currently hold the position of researcher with tenure at Politecnico di Milano, within the Dipartimento di Elettronica, Informazione e Bioingegneria. My research interests focus on the interaction between compiler and computer architecture, including compilation technologies for enforcing extra-functional properties such as performance, energy-efficiency, and security. Therefore, I participate in both the Advanced software architectures and methodologies and the System Architectures research lines within the Computer Science and Engineering section of the department.
I am a founding member of the HEAP Laboratory, where I lead a research team composed of three post-doctoral researchers, three doctoral students and several master's student.

Career Highlights

My paper "Compiler-based Techniques to Secure Cryptographic Embedded Software against Side Channel Attacks" has appeared in the *Top Picks in Hardware and Embedded Security 2012-2017* special issue of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Furthermore, I have received *two best paper awards*, one of which from a conference sponsored by the ACM SIGAPP, and one best poster award from a conference sponsored by the ACM SIGMICRO. I have been a member of the HiPEAC Network of Excellence since 2007, and have been awarded the "HiPEAC Paper Award" [1] four times, for papers published at the Design Automation Conference, a top-ranked conference.

I have participated to 10 European projects, which obtained a total funding of over 36 M€. Activities directly managed by me (leading up to 20 partners from all around Europe), as Task leader, Workpackage leader, Project Technical Manager, or responsible for the local unit, accounted for a total

[1] The "HiPEAC Paper Award" is given in recognition of publications in top conferences in the Compilers and Computer Architectures areas, where the presence of European researchers is considered low.

funding of over 7.5 M€, of which over 1.8 M€ funding activities carried out by Politecnico di Milano.

I am Associate Editor of SoftwareX, an international peer-reviewed journal published by Elsevier and currently ranked in the first quartile of the Scimago ranking.

Research Vision Statement

Compiler technology is often considered a commodity, and therefore not at the forefront of research. While it is accurate to say that the field is mature, there is still a wide demand for better compilers, and a wide range of opportunities for major advances. In particular, commodity compilers only address to a marginal extent extra-functional properties of hardware/software systems other than performance. Indeed, important system properties such as energy efficiency and security are not satisfactorily addressed. *Thus, my primary research goal is to enlarge the range of extra-functional properties that can be optimized or enforced automatically through compiler transformations and analyses.*

Compiler Techniques for Hardening Cryptographic Primitives Implementations

An area where compilers can prove invaluable is that of protecting the software implementation of cryptographic primitives from attacks that exploit information leakage from side channels such as timing, power consumption, or electromagnetic emissions.
The precise quantification of information leakage is difficult to perform by hand, but, in collaboration with colleagues from the Applied Cryptography group (Prof. Gerardo Pelosi and Prof. Alessandro Barenghi), we were able to define a *Security-Oriented Dataflow Analysis* (SDFA) which can precisely identify, down to the individual bit level, which intermediate values of a computation are vulnerable to side channel analysis [C36, C40].
Based on the SDFA, it was then possible to define several protection strategies that can be applied automatically through the compiler [J12, J14, C37, C38, C46], as well as some that employ self-modifying code as part of the defense [J11, C39]. Finally, to provide a full engineering approach, the SDFA was used as part of a secure-by-design methodology for the design of encryption solutions [J9, O3]. Our seminal work on the application of compiler techniques to side channel countermeasures [C32] has been selected among the Top Picks in Hardware and Embedded Security (2012-2017), and our account of the evolution of that work has been published in the corresponding special issue of the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems [J18].

Compiler Techniques for Energy Efficiency & Performance

Achieving energy efficiency through compiler transformations (and possibly through co-designing such transformations with the hardware architecture) is still an open problem for all kinds of computing systems, from embedded to high performance ones.
During the past years, I tackled several aspects of this problem, starting from the automated application and optimization of *memoization*, an approach to trade off memory space and computation time which is applicable to pure functions. Through a collaboration with the team led by Prof. Chiara Francalanci (Information Systems area), a compiler-based approach for Java applications was developed [J7, C26, O2].
A second line of work towards improving energy efficiency is that of compiler-architecture co-optimization [J2, J8]. I started the investigation on this topic by devising a method for modelling the performance impact of compiler and architecture parameters [J3], in collaboration with Prof. Cristina Silvano and Prof. Gianluca Palermo. Then, through a collaboration with the PULP team

led by Prof. Luca Benini at ETH Zürich, we were able to co-design the compiler and the architecture of an OpenRISC core, with significant benefits [C49].
Recently, I started investigating compiler-based approaches to *approximate computing*, in the context of the H2020 ANTAREX project [C64]. In collaboration with the INRIA Rennes PACAP team, led by Dr. Erven Rohou, we obtained initial results on applying precision reduction to High Performance Computing (HPC) applications [C65], while with the Universidade do Porto team of Prof. João Cardoso we are working on applying precision tuning to heterogeneous architectures [C66]. The research has led to the creation of the *TAFFO* set of plugins for LLVM [J19, C68, O14].

Dynamic Compilation

Dynamic compilation is a key technique to exploit at compiler level runtime information. I have explored dynamic compilation techniques in conjunction with Very Long Instruction Word (VLIW) architectures [J1, C4, C8], providing VLIW scheduler designs for a Java Virtual Machine, under the supervision of Prof. Stefano Crespi Reghizzi. This research line led to the design of a Java Virtual Machine with a very small footprint for use in embedded devices [C9], as well as to the design of optimized selective compilation techniques (a.k.a. *hotspot*) [C7].
The study of the dynamic compilation process further led to the design of techniques for exploiting parallelism to hide compilation latencies, as well as to the implementation of such techniques in a dynamic compiler for Microsoft's CIL bytecode [J6, C19, C16, C25, O1].
More recently, with a doctoral student, Stefano Cherubin (2016-2019), I revived this research line by investigating the applicability of partial dynamic compilation techniques in environments where dynamic compilers are not available or not desired for the entire application (e.g., HPC production environments) [J16, C68].

Reverse Engineering

Reverse engineering is a key technique for malware and binary analysis as well as for legacy code support, via binary-to-binary translation. In this field I supervised a very successful doctoral student, Alessandro Di Federico (2015-2017), whose work on fundamental techniques obtained good results through an innovative approach leveraging open source components such as QEMU and LLVM [C56], and I am supervising another, Andrea Gussoni, whose activities focus on the exploitation of the research potential of the tool [C69]. This activity included a collaboration with Purdue University [C61], and resulted in an open source tool, REVAMB.
The current research direction along this line involves extending the ability of the reverse engineering tool to operate as a binary-to-binary compiler, in collaboration with a startup company, Rev.ng srls.

Parallel Programming Models & Applications

Since automatic parallelisation is still far from effective, parallel programming models are key to achieving high performance, especially in heterogeneous systems. In collaboration with doctoral students and colleagues in the HEAP Laboratory, I co-designed one of the first solutions for parallel execution of the AES encryption primitive on CUDA-enabled General Purpose Graphics Processing Units (GPGPUs) [C20]. From this seminal work, we developed record-setting solutions for several encryption standards and security applications [C18, C22, C33, C34], and finally gathered the collected knowledge about the impact of architectural features on performance [J10].
Beyond the development of parallel applications, I also investigated the efficient implementation of programming models such as OpenCL [B2, C28, C47, C55, C23] and OpenMP [C30, C27]. Most recently, I designed and implemented a simple parallel programming model, the MANGO API, for use in High Performance Computing (HPC), characterised by the ability to integrate runtime-resource management. This programming model has been integrated with resource management techniques

in collaboration with the research team of Prof. William Fornaciari [J17, C63, C57, O9]. This result integrates a series of ideas on resource management of parallel computing systems previously developed in collaborative research projects [C41, C44, C43, C62].
The current research direction along this line is to extend the programming model to provide support for predictability of performance in HPC systems, including performance portability across heterogeneous accelerators [O15].
I have recently started, in collaboration with Prof. Francesco Casella and Prof. Alberto Leva, and a team of research associates and doctoral and master students, the investigation of the design of an efficient and effective compiler for the Modelica language for the simulation of dynamic systems characterised by differential equation systems coupled with digital components [C67].

Embedded & Cyber-Physical Systems Design

While my interests revolve primarily around compiler technologies, I have been also involved in several research activities related to the design of embedded systems [B4, O6, J15], including Internet of Things applications [J13, B5, O8, O12] and cyber-physical systems [C45] (the latter in collaboration with the Human-Computer Interaction team led by Prof. Franca Garzotto), with an emphasis on the security aspects of such systems [C42, O4].
The current research direction along this line is focused on the application of secure and fast encryption techniques as well as of approximate computing strategies to specific embedded solutions.

Electronic Design Automation

EDA tools and techniques are closely related to compilers. Therefore, there is often the opportunity to apply compiler technology to the analysis or synthesis of hardware specifications. In an early collaboration with Prof. Donatella Sciuto's group, I developed techniques for static analysis of transaction-level models [J4, C1], including UML-based modeling [B1] and adaptive metrics for functional partitioning [C10] (the latter in cooperation with Prof. Marco Santambrogio and with Prof. Seda Ogrenci Memik of Northwestern University).
With Prof. Francesco Bruschi and Prof. Gerardo Pelosi, we then provided a new insight, and related tools, on the nature of the *Boolean matching* problem in logic synthesis [J5, C14, C13].

Habilitation for the position of Associate Professor

2019-2025 Settore concorsuale *09/H1*, Sistemi di Elaborazione dell'Informazione (Computer Engineering).
2017-2023 Settore concorsuale *01/B1*, Informatica (Computer Science).

Appointments held

2008-current Researcher with tenure, DEIB, Politecnico di Milano, Milano, Italy.
2005-2008 Researcher, DEI, Politecnico di Milano, Milano, Italy.
2004 Research Associate (Assegnista di Ricerca), DEI, Politecnico di Milano, Milano, Italy.
Title of grant: "Compilazione e schedulazione dinamica per macchine VLIW" (Dynamic compilation and scheduling for VLIW architectures).
2001-2004 PhD Student, DEI, Politecnico di Milano, Milano, Italy.
1999-2000 Intern, Advanced Systems Technology group, STMicroelectronics, Agrate Brianza (MB), Italy.
Assignment: design and implementation of an algorithm for parallelizing C code to be compiled for a cluster of ILP processors.

Education

2004 PhD in Information Technology, Politecnico di Milano.
Dissertation: "Dynamic Compilation for Architectures supporting Instruction Level Parallelism".
Advisor: Prof. Stefano Crespi Reghizzi.

2000 Laurea in Ingegneria Informatica (V.O.), Politecnico di Milano.
Thesis: "Tecniche avanzate di compilazione applicate a macchine parallele e riconfigurabili" (Advanced Compilation Techniques for Parallel and Reconfigurable Architectures).
Advisor: Prof. Stefano Crespi Reghizzi.
Co-Advisor: Rinaldo Poluzzi, AST, STMicroelectronics.

1994 Maturità classica, Liceo Ginnasio Giuseppe Parini, Milano.

Honors & awards

I have been a member of the HiPEAC Network of Excellence since 2007, and have been awarded the "HiPEAC Paper Award" four times. The "HiPEAC Paper Award" is given in recognition of publications in top conferences in the Compilers and Computer Architectures areas, where the presence of European researchers is considered low.
Furthermore, I have received two best paper awards, one of which from a conference sponsored by the ACM SIGAPP, as well as one best power award from a conference sponsored by the ACM SIGMICRO.
One of my papers [C32] has been selected as a Top Pick in Hardware and Embedded Security 2012-2017 [J18].

2019 Best Poster Award at ACM International Conference on Computing Frontiers, for the poster Fixed Point Exploitation via "Compiler Analyses and Transformations".

2018 Selected among the Top Picks in Hardware and Embedded Security (2012-2017) for "A code morphing methodology to automate power analysis countermeasures", appeared at DAC 2012.

2018 Bronze Medal as the coach of a team classifying 9th in the regional qualifications for the International Collegiate Programming Contest in the South-Western Europe Region, a global competition of programming for undergraduate student teams.

2015 "HiPEAC Paper Award" for the paper "Information leakage chaff: feeding red herrings to side channel attackers" appeared at DAC 2015.

2014 "HiPEAC Paper Award" for the paper "A Multiple Equivalent Execution Trace Approach to Secure Cryptographic Embedded Software" appeared at DAC 2012.

2014 Best Paper Awards (Overall and Cryptographic Techniques) at the SIN 2014 conference for the paper "Differential Fault Analysis for Block Ciphers: an Automated Conservative Analysis".

2013 "HiPEAC Paper Award" for the paper "Compiler-based side channel vulnerability analysis and optimized countermeasures application" appeared at DAC 2013.

2012 "HiPEAC Paper Award" for the paper "A code morphing methodology to automate power analysis countermeasures" appeared at DAC 2012.

Best Paper Award (Applications area) at the ACM SAC 2008 conference for the paper "Dynamic Configuration of Application-Specific Implicit Instructions for Embedded Pipelined Processors".

2007–current Member of the High Performance & Embedded Architectures and Compilers (HiPEAC) Network of Excellence.

Research Activities

I have been involved in funded research projects since 2004, participating to 10 European projects, which obtained a total funding of over 36 M€, of which a total of over 4 M€ funded activities carried out by Politecnico di Milano. More specifically, activities directly managed by me, as Task leader, Workpackage leader, Project Technical Manager, or responsible for the local unit, accounted for a total funding of over 7.5 M€, of which over 1.8 M€ funding activities carried out by Politecnico di Milano.
Furthermore, as a Workpackage leader I managed activities involving at the same time up to 20 partners from all around Europe.
I have also been involved in the development of the project proposals for all the projects in which I have participated, except for ICODES, and have in particular been among the primary authors for the RECIPE, ANTAREX, and 2PARMA proposals.
The 2PARMA project was also deemed a *success story* by the European Commission. I have also co-represented the RECIPE project at the FETHPC Cluster Meeting held by the European Commission DG-CONNECT.

Participation to and Management of Funded Research Projects

2018-current H2020 FET-HPC RECIPE
Coordinator: Prof. William Fornaciari, Politecnico di Milano.
Role: Project Technical Manager, responsible for all scientific and technical developments.
Total EU contribution 3.28 M€, of which 0.705 M€ to Politecnico di Milano.
EU contribution to managed activities: 3.28 M€, of which 0.705 M€ to Politecnico di Milano.

2018-2019 Regione Lombardia, call "Progettare la parità in Lombardia 2018", Il filo di Arianna – Ariadne's thread
Coordinator: Claudia Di Palma, SVS Donna Aiuta Donna ONLUS
Role: Responsible for local unit.
Total Regione Lombardia contribution 15 k€.

2016-2019 H2020 ICT-04 Modular Microserver DataCentre (M2DC), project id 688201
Coordinator: Dr. Ariel Oleksiak, Poznan National Supercomputing Center, Poland.
Role: participant to Tasks 1.1 (Application Requirements) and T6.4 (Internet of Things Data Analytics).
Total EU contribution: 8 M€ of which 0.25 M€ to Politecnico di Milano .

2016-2019 ECSEL JU Safe Cooperating Cyber-Physical Systems (SafeCOP), project id 100230.
Coordinator: Detlef Scholle, Alten Sweden AB.
Role: Task leader for Task 5.5, responsible for the vehicle-to-infrastructure for traffic management use case.
Total EU contribution 3.78 M€, of which 0.125 M€ to Politecnico di Milano.
EU contribution to managed tasks: 0.334 M€, of which 0.035 M€ to Politecnico di Milano.

2015-2019 H2020 FET-HPC AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems (ANTAREX), project id: 671623.
Coordinator: Prof. Cristina Silvano, Politecnico di Milano.
Role: Task leader for Task 1.2, responsible for the specification of APIs and tools and T2.5, responsible for domain specific language features for extra-functional characteristics.
Total EU contribution 3.11 M€ of which 0.577 M€ to Politecnico di Milano.
EU contribution to managed tasks: 0.130 M€, of which 0.05 M€ to Politecnico di Milano.

2015-2019 H2020 FET-HPC MANGO: exploring Manycore Architectures for Next-GeneratiOn HPC systems, project id 671668.
Coordinator: Prof. José Flich Cardo, Universitat Politecnica de Valencia.
Role: Workpackage leader for WP2, responsible for the software stack development including compilers, programming models, and runtime resource management.
Total EU contribution: 5.8 M€, of which 0.646 M€ to Politecnico di Milano .
EU contribution to managed workpackage: 1.1 M€, of which 0.331 M€ to Politecnico di Milano.

2015 EIT Digital Program 2015, Playful Supervised Smart Spaces (P3S).
Coordinator Prof. Franca Garzotto, Politecnico di Milano.
Role: Scientific responsibility for the local unit for Task A1501 (Smart Objects) responsible for the development of smart connected objects.
Total EIT contribution: 0.65 M€, of which 0.15 M€ to Politecnico di Milano. EIT contribution managed: 23 k€.

2010-2013 FP7-ICT PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures (2PARMA), project id 248716.
Coordinator: Prof. Cristina Silvano, Politecnico di Milano.
Role: Workpackage leader for WP2, responsible for compiler and OpenCL support development.
Total EU Contribution 2.741 M€ of which 0.545 M€ to Politecnico di Milano.
EU contribution to managed workpackage: 0.51 M€ of which 0.154 M€ to Politecnico di Milano.

2010-2013 ARTEMIS JU Smart Multicore Embedded SYstems (SMECY), project id 100230.
Coordinator: Dr. François Pacull, CEA LETI, France.
Role: Workpackage leader for WP3, responsible for the development of optimization techniques, programming model support, and fault tolerance.
Total EU contribution 3.27 M€, of which 0.25 M€ to Politecnico di Milano.
EU contribution to managed workpackage: 1.2 M€, of which 0.25 M€ to Politecnico di Milano.

2008-2009 FP7-ICT OpenMediaPlatform, project id 214009.
Coordinator: Prof. Stefano Crespi Reghizzi, Politecnico di Milano.
Role: Workpackage leader for WP2, responsible for dynamic compiler development.
Total EU Contribution 3.27 M€ of which 0.545 M€ to Politecnico di Milano.
EU contribution to managed workpackage: 0.95 M€ of which 0.27 M€ to Politecnico di Milano.

2004-2007 FP6-IST Interface- and Communication based Design of Embedded Systems, project id 004452.
Coordinator: Prof. Jens-E. Appel, OFFIS, Germany.
Role: Co-author of one deliverable on requirements on metrics for early communication cost estimation.
Total EU Contribution 2.85 M€, of which 0.27 M€ to Politecnico di Milano .

Other International Collaborations

In addition to international collaborations based on funded projects, I have also opened the following international research collaborations.

2016 Collaboration with Prof. Mathias Payer of Purdue University on reverse engineering techniques. One of the doctoral students under my supervision visited Purdue, resulting in a joint publication [C61].

Development of compiler support and optimizations for the Open Hardware processor PULP, designed by ETH Zürich and Universitá degli Studi di Bologna. My team cooperated with the hardware design group led by Prof. Luca Benini, for an effective co-design of instruction set architecture and compiler [C49].

Teaching and Supervision Activities

I have taught Compiler Construction courses at the graduate level since 2013, as well as a variety of courses at both the graduate and undergraduate level on algorithmics, system software design, and foundations of computer science. I have also taught a course on energy-aware computing within the doctoral program in Information Technology.
I have been advisor of three doctoral students, co-advisor of three, and I am currently supervising three more.
I am also supervising the research activities of one post-doctoral research associates, and have supervised or co-supervised three more.

Supervision of Post-Doctoral research activities

2019-current Supervisor of post-doctoral research activities ("assegno di ricerca") for dr. Stefano Cherubin.
2018-2019 Supervisor of post-doctoral research activities ("assegno di ricerca") for dr. Alessandro Di Federico.
2018-2019 Supervisor of post-doctoral research activities ("assegno di ricerca") for dr. Pietro Fezzardi.
2013-2015 Co-supervisor (with Prof. Luca Breveglieri) of post-doctoral research activities ("assegno di ricerca") for dr. Alessandro Barenghi.

Supervision of Doctoral and Master's studies

2019-current Advisor for the doctoral studies of Daniele Cattaneo, PhD program in Information Technology, XXXV cycle, Politecnico di Milano.
Topic of research: compiler support for approximate computing.
2018-current Advisor for the doctoral studies of Andrea Gussoni, PhD program in Information Technology, XXXIV cycle, Politecnico di Milano.
Topic of research: Reverse engineering through binary code decompilation.
2017-current Advisor for the doctoral studies of Anna Pupykina, PhD program in Information Technology, XXXII cycle, Politecnico di Milano.
Topic of research: Resource and memory management in deeply heterogeneous HPC systems.
2016-2019 Advisor for the doctoral studies of dr. Stefano Cherubin, PhD program in Information Technology, XXXI cycle, Politecnico di Milano.
Title of dissertation: "Compiler-Assisted Dynamic Precision Tuning".
First employment after achieving the doctoral degree: Research Associate at Politecnico di Milano.
2015-2017 Advisor for the doctoral studies of dr. Alessandro Di Federico, PhD in Information Technology, XXX cycle, Politecnico di Milano.
Title of dissertation: "Compiler Techniques for Binary Analysis and Hardening".
First employment after achieving the doctoral degree: Research Associate at Politecnico di Milano & Founder at Rev.ng Srls.
2013-2015 Advisor for the doctoral studies of dr. Michele Scandale, PhD in Information Technology, XXVIII cycle, Politecnico di Milano.
Title of dissertation: "Towards Improving Programmability of Heterogeneous Parallel Architectures".
First employment after achieving the doctoral degree: Compiler Engineer at Apple.
2011-2013 Co-Advisor of the doctoral studies of dr. Marco Bessi (Advisor: Prof. Chiara Francalanci), PhD in

Information Technology, XXVI cycle, Politecnico di Milano.
Title of Dissertation: "A Methodology to Improve the Energy Efficiency of Software"
First employment after achieving the doctoral degree: Solution Delivery Consultant at CAST.

2010-2012 Co-Advisor of the doctoral studies of dr. Ettore Speziale (Advisor: Prof. Stefano Crespi Reghizzi), PhD in Information Technology, XXV cycle, Politecnico di Milano.
Title of Dissertation: "Improving Synchronization and Data Access in Parallel Programming Models".
First employment after achieving the doctoral degree: Compiler Engineer at ARM Ltd.

2008-2012 Co-Advisor of the doctoral studies of dr. Andrea Di Biagio, PhD in Information Technology, XXIII cycle, Politecnico di Milano (Advisor: Prof. Stefano Crespi Reghizzi).
Title of Dissertation: "Synchronization Optimization for Distributed Shared Memory Multiprocessors".
First employment after achieving the doctoral degree: Compiler Engineer at Sony SN Systems.

2004-current Advisor of theses for the degree of Master of Science in Computer Engineering at Politecnico di Milano (10+ in the last 5 years).

2003 Mentor for the Master of Engineering in Embedded Systems Design thesis of Prasad Balasubramanian, "Impact of source code specialization on energy and performance of software", Advanced Learning and Research Institute, Università della Svizzera Italiana, Lugano (CH).

Membership in revision committees for Doctoral Candidates

2016-current Member of revision committee (external examiner) for the doctoral studies of Pedro Miguel dos Santos Pinto, at Faculty of Engineering of the University of Porto, Portugal.

2007 Member of revision committee (controrelatore) for the doctoral studies of Alberto Gallini, at Università di Milano Bicocca.

Courses

2013-current Code Transformation and Optimization, within the Master of Science in Computer Engineering (Laurea Specialistica in Ingegneria Informatica) at Politecnico di Milano.

2019 "Reviewing the Literature: Building a State of the Art", within the "Passion in Action" extra-curricular innovative teaching program for Engineering students at Politecnico di Milano (all levels from undergraduates to doctoral students), in collaboration with Dr. Francesca M. Rossi.

2018-2019 "Introduzione alla programmazione in Python" (introduction to programming in Python), within the extra-curricular innovative "Passion in Action" teaching program for Engineering students at Politecnico di Milano (all levels from undergraduates to doctoral students), in collaboration with Dr. Francesco Bruschi.

2016 "Energy aware design of computing systems and applications", within the doctoral program in Information Technology at Politecnico di Milano, as the primary organizer (with Prof. William Fornaciari as co-organizer).

2014 "Energy aware design of computing systems and applications", within the doctoral program in Information Technology at Politecnico di Milano, as a co-organizer with Prof. William Fornaciari.

2012 The 2PARMA OpenCL Compiler Toolchain, at the Fall School on Programming Paradigms for Multicore Embedded Systems, Oct 2012, Freudenstadt, Germany (with Michele Scandale).

2011-2012 Piattaforme Software per la Rete (software platforms for networking) within the Laurea in Ingegneria Informatica and Laurea in Ingegneria delle Telecomunicazioni (Computer Engineering and Telecommunications Engineering, undergraduate programs) at Politecnico di Milano.

2010 Algoritmi e Principi dell'Informatica (principles of algorithms and data structures) within the Laurea in Ingegneria Informatica (Computer Engineering, undergraduate program) at Politecnico di Milano.

2007-2010 Informatica 3 (principles of programming language design, algorithms and data structures) within the Laurea in Ingegneria Informatica (Computer Engineering, undergraduate program) at Politecnico di Milano.

2005-2010 Laboratorio Software (software design and operating systems laboratory) within the Laurea Specialistica in Ingegneria Informatica (Computer Engineering, graduate program) at Politecnico di Milano.

2004 Informatica C (fundamentals of computer programming and architecture) within the Laurea in Ingegneria Chimica e dei Materiali (Chemical Engineering, undergraduate program) at Politecnico di Milano.

Other Teaching Activities

2001-current Teaching Assistant at Politecnico di Milano for the courses of foundations of computer science (undegraduate programs in Computer Engineering, Telecommunication Engineering, Mathematical Engineering, and Chemistry and Materials Sciences).

2013-current Teaching Assistant at Politecnico di Milano for the courses of Advanced Computer Architectures (graduate program in Computer Engineering).

2002-2006 Teaching Assistant at Politecnico di Milano for the courses of High Performance Processors (graduate program in Computer Engineering in conjunction with University of Illinois at Chicago).

2002-2007 Teaching Assistant at Politecnico di Milano for the courses of Formal Languages and Compilers (graduate program in Computer Engineering).

Service Activities

I am currently Associate Editor of SoftwareX (Elsevier, SJR Q1), as well as Guest Editor for a special issue of Parallel Computing (Elsevier, SJR Q2) and for a special issue of Security and Communication Networks (Wiley/Hindawi, SJR Q2).

I am/have been a member of the program committee of several conferences and workshops, including Euro-Par, NTMS, SAMOS, and the special session on European Projects at DATE.

I coach the undergraduate teams from Politecnico di Milano participating to the International Collegiate Programming Competition (ICPC). In 2018, me and my top-performing team have been awarded the Bronze Medal at the South-West Europe regional qualifications.

Organisation of Scientific Conferences and Workshops

2019 Member of the program committee for the Euro-Par 2019.

2018 Member of the program committee for the IFIP International Conference on New Technologies, Mobility & Security (NTMS 2108).

2018 Member of the program committee for the 14th International Workshop on Scheduling and Resource Management for Parallel and Distributed Systems (SRMPDS2018).

2017 Member of the program committee for the 1st Workshop on Autotuning and Adaptivity Approaches for Energy Efficient Systems (ANDARE), held in conjunction with the 26th International Conference on Parallel Architectures and Compilation Techniques (PACT).

2016-current Member of the program committee of the International Workshop on High Performance Energy Efficient Embedded Systems (HiP3ES).

2016-2017 Member of the program committe for the Design Automation and Test in Europe (DATE), Special Track on EU Projects.

2015-current Member of the program committee of the Euromicro Conference on Digital System Design, for the Special Session on Architectures and Hardware for Security Applications.

2015 Member of the program committee of the International Workshop on Architecture-Aware Simulation and Computing.

2014-current Member of the organizing and program committee of the Workshop on Cryptography and Security in Computing Systems (CS^2), co-located with the HiPEAC Conference (founding member).
The proceedings of the CS^2 workshop are published in the ACM International Conference Proceedings Series.

2014-current Member of the program committee of the International Conference on Embedded Computing Systems: Architectures, Modeling and Simulation (SAMOS XVI).

2011 Finance Chair for the Architecture of Computing Systems (ARCS 2011) conference.

2010-current Member of the organising and program committees for the Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures (PARMA) (founding member) and of the Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms (DITAM) (starting from the third edition, held jointly with the PARMA workshop), co-located with the HiPEAC Conference (and, for the 1st and 2nd PARMA Workshop only, with the ARCS conference).
Program Chair in 2016 and 2017.
General Chair in 2015.
The proceedings of the PARMA-DITAM workshop are published in the ACM International Conference Proceedings Series.

2008 Local arrangements Co-Chair for the 41st IEEE/ACM MICRO Conference.

Participation to Editorial Boards, Revision of Scientific Articles and Project Proposals

2019-current Associate Editor for SoftwareX (Elsevier).

2018-2019 Guest Editor for Parallel Computing (Elsevier), Special Issue on Programming, Resource Management and Autotuning Tools for Heterogeneous HPC (with Dr. Antonino Tumeo, Pacific Northwest National Laboratory, USA).

2018-2019 Lead Guest Editor for Security and Communication Networks (Wiley/Hindawi), Special Issue on Advances in Cryptography and Security in Computing Systems (with Prof. Karine Heydemann, Sorbonne Université, France; Prof. Nicolas Sklavos, University of Patras, Greece; and Prof. Leonel Sousa, INESC-ID Universidade de Lisboa, Portugal).

2017 Rapporteur (responsible for the consensus report) and reviewer for the COST (European Cooperation in Science and Technology) Association Open Call OC-2016-2.

2015 Reviewer for two project proposals for the 1/2016 Academic Research Fund Tier 2 Grant Call MOE2015-T2-2 of the Singapore Ministry of Education.

2011 Evaluator for the CHIST-ERA (European Coordinated Research on Long-term Challenges in Information and Communication Sciences & Technologies) Call 2011.

2010-current Reviewer of scientific articles for several international journals, including: ACM Transactions on Architectures and Code Optimization; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Microprocessors and Microsystems (Elsevier); IEEE Transactions on Computers.

Other Service Activities

2016-current Mentoring of student teams to the International Collegiate Programming Competition. Starting in 2017, I also organised the local selections (involving circa 100 students per year) for the Politecnico di Milano teams for the regional competition. Me and my top-performing team have been awarded the *Bronze Medal* in the 2018 South-West Europe regional competition.

2011-current Member of the logistics board of the School of Industrial and Computer Engineering, Politecnico

di Milano.

2001-2002 Elected representative of the doctoral students to the Department council of DEIB, Politecnico di Milano.

Publications & Talks

I have published a total of 19 articles in scientific journals with international peer-review committees, as well as 5 book chapters and 70 papers in conferences and workshops with international peer-review committees.
Finally, I have also held three invited talks, one at the 18th IEEE Conference on Computational Science and Engineering, and two at the HiPEAC Virtualization Cluster Meeting.

Bibliometrics:

Google Scholar citations 1004, h-index 18

Scopus citations 598, h-index 13

According to CSRankings[2], 6 of my publications contribute to Politecnico di Milano position as second institution in Europe on Design Automation (top contributor on par with Gerardo Pelosi when considering the last 15 years, second contributor after Donatella Sciuto when considering no time boundaries).
According to SciVal[3], for the last five years, my publications have a field-weighted citation impact of 1.67 (i.e., are cited 67% more than expected for the research area). For my overall career, the same metric is 1.48, indicating that my publications have achieved an increased impact in the last years.
Considering recent publications, over 35% have been authored in collaboration with international partners, and over 18% included an industrial collaboration, including companies such as Thales Communications & Security, ARM Ltd, Philips HealthTech, STMicroelectronics, Synopsys, Vodafone Automotive, Dompé Farmaceutici, Eaton Industries, Alten.

International Journal articles

[J1] G. Agosta, S.C. Reghizzi, G. Falauto, and M. Sykora. JIST: Just-In-Time scheduling translation for parallel processors. *Scientific Programming*, 13(3):239–253, 2005.

[J2] Giovanni Agosta, Luca Breveglieri, Gerardo Pelosi, and Martino Sykora. Programming Highly Parallel Reconfigurable Architectures for Symmetric and Asymmetric Cryptographic Applications. *Journal of Computers*, 2(9):50–59, 2007.

[J3] Cristina Silvano, Giovanni Agosta, and Gianluca Palermo. Efficient architecture/compiler co-exploration using analytical models. *Design Automation for Embedded Systems*, 11(1):1–23, 2007.

[J4] Giovanni Agosta, Francesco Bruschi, and Donatella Sciuto. Static analysis of transaction-level communication models. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(8):1412–1424, 2008.

[J5] Giovanni Agosta, Francesco Bruschi, Gerardo Pelosi, and Donatella Sciuto. A transform-parametric approach to boolean matching. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 28(6):805–817, 2009.

[2] CSRankings measures the number of contributions to the most selective conferences in each area of computer science.
[3] SciVal is Elsevier's research intelligence tool. The metrics provided are computed on Scopus data, as of 2018.

[J6] Simone Campanoni, Giovanni Agosta, Stefano Crespi Reghizzi, and Andrea Di Biagio. A highly flexible, parallel virtual machine: design and experience of ILDJIT. *Software: Practice and Experience*, 40(2):177–207, 2010.

[J7] Giovanni Agosta, Marco Bessi, Eugenio Capra, and Chiara Francalanci. Automatic memoization for energy efficiency in financial applications. *Sustainable Computing: Informatics and Systems*, 2(2):105–115, 2012.

[J8] Andrea Di Biagio, Giovanni Agosta, Martino Sykora, and Cristina Silvano. Architecture optimization of application-specific implicit instructions. *ACM Transactions on Embedded Computing Systems (TECS)*, 11(SUPPL. 2), 2012.

[J9] Giovanni Agosta, Alessandro Barenghi, Massimo Maggi, and Gerardo Pelosi. Design space extension for secure implementation of block ciphers. *IET Computers & Digital Techniques*, 8(6):256–263, 2014.

[J10] Giovanni Agosta, Alessandro Barenghi, Alessandro Di Federico, and Gerardo Pelosi. OpenCL performance portability for general-purpose computation on graphics processor units: an exploration on cryptographic primitives. *Concurrency Computation*, 27(14):3633–3660, 2015.

[J11] Giovanni Agosta, Alessandro Barenghi, Gerardo Pelosi, and Michele Scandale. The MEET Approach: Securing Cryptographic Embedded Software Against Side Channel Attacks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 34(8):1320–1333, 2015.

[J12] Giovanni Agosta, Alessandro Barenghi, Gerardo Pelosi, and Michele Scandale. Trace-based schedulability analysis to enhance passive side-channel attack resilience of embedded software. *Information Processing Letters*, 115(2):292–297, 2015.

[J13] A. Oleksiak, M. Kierzynka, W. Piatek, G. Agosta, A. Barenghi, C. Brandolese, W. Fornaciari, G. Pelosi, M. Cecowski, R. Plestenjak, J. Činkelj, M. Porrmann, J. Hagemeyer, R. Griessl, J. Lachmair, M. Peykanu, L. Tigges, M.V.D. Berge, W. Christmann, S. Krupop, A. Carbon, L. Cudennec, T. Goubier, J.-M. Philippe, S. Rosinger, D. Schlitt, C. Pieper, C. Adeniyi-Jones, J. Setoain, L. Ceva, and U. Janssen. M2DC – Modular Microserver DataCentre with heterogeneous hardware. *Microprocessors and Microsystems*, 52:1339–1351, 2017.

[J14] Giovanni Agosta, Alessandro Barenghi, Gerardo Pelosi, and Michele Scandale. Reactive Side-channel Countermeasures: Applicability and Quantitative Security Evaluation. *Microprocessors & Microsystems*, 2018. accepted July 4, 2018.

[J15] Ali Balador, Anis Kouba, Dajana Cassioli, Fotis Foukalas, Ricardo Severino, Daria Stepanova, Giovanni Agosta, Jing Xie, Luigi Pomante, Maurizio Mongelli, Pierluigi Pierini, Stig Petersen, and Timo Sukuvaara. Wireless Communication Technologies for Safe Cooperative Cyber Physical Systems. *Sensors*, 18, 2018.

[J16] Stefano Cherubin and Giovanni Agosta. libversioningcompiler: An easy-to-use library for dynamic generation and invocation of multiple code versions. *SoftwareX*, 7:95 – 100, 2018. Elsevier.

[J17] José Flich, Giovanni Agosta, et al. MANGO: exploring Manycore Architectures for Next-GeneratiOn HPC systems. *Microprocessors & Microsystems*, 61:154 – 170, 2018.

[J18] Giovanni Agosta, Alessandro Barenghi, and Gerardo Pelosi. Compiler-based techniques to secure cryptographic embedded software against side channel attacks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pages 1–5, 2019.

[J19] Stefano Cherubin, Daniele Cattaneo, Michele Chiari, Antonio Di Bello, and Giovanni Agosta. TAFFO: Tuning assistant for floating to fixed point optimization. *IEEE Embedded Systems Letters*, pages 1–4, 2019.

International Book Chapters

[B1] Giovanni Agosta, Francesco Bruschi, and Donatella Sciuto. UML Tailoring for SystemC and ISA Modelling. *UML for SOC Design*, pages 147–173, 2005.

[B2] C. Silvano, W. Fornaciari, S.C. Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A. Di Biagio, E. Speziale, M. Tartara, D. Melpignano, J.-M. Zins, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Leupers, H. Meyr, J. Ansari, P. Mahonen, and B. Vanthournout. 2PARMA: Parallel paradigms and run-time management techniques for many-core architectures. In *Designing Very Large Scale Integration Systems: Emerging Trends & Challenges*, volume 105 LNEE, pages 65–79, 2011.

[B3] Giovanni Agosta, Alessandro Barenghi, Gerardo Pelosi, and Michele Scandale. Symmetric Key Encryption Acceleration on Heterogeneous Many-Core Architectures. *Practical Cryptography: Algorithms and Implementations Using C++*, pages 251–297, 2014. ISBN 978-1-4822-2889-2.

[B4] Giovanni Agosta, Mickael Cartron, and Antonio Miele. Fault tolerance. In *Smart Multicore Embedded Systems*, volume 9781461488002, pages 81–101. Springer, 2014.

[B5] Ariel Oleksiak, Michal Kierzynka, Wojciech Piatek, Micha Vor Dem Berge, Wolfgang Christmann, Stefan Krupop, Mario Porrmann, Jens Hagemeyer, René Griessl, Meysam Peykanu, Lennart Tigges, Sven Rosinger, Daniel Schlitt, Christian Pieper, Udo Janssen, Giovanni Agosta, Carlo Brandolese, William Fornaciari, Gerardo Pelosi, Mariano Cecowski, Robert Plestenjak, Justin Cinkelj, Loic Cudennec, Thierry Goubier, Jean-Marc Philippe, Chris Adeniyi-Jones, Luca Ceva, and Holm Rauchfuss. M2DC – Modular Microserver DataCentre with Heterogeneous Hardware. In *Data Center Accelerators for Cloud Computing*, pages 109–128. Springer publication, 2018.

International Conference and Workshop Papers

[C1] Giovanni Agosta, Francesco Bruschi, and Donatella Sciuto. Static analysis of transaction-level models. In *Proceedings of the 40th annual Design Automation Conference*, pages 448–453. ACM, 2003.

[C2] Giovanni Agosta, Francesco Bruschi, and Donatella Sciuto. Synthesis of dynamic class loading specifications on reconfigurable hardware. In *Second IEEE International Workshop on Electronic Design, Test and Applications, Proceedings. DELTA 2004.*, pages 431–433. IEEE, 2004.

[C3] Giovanni Agosta, Gianluca Palermo, and Cristina Silvano. Multi-objective co-exploration of source code transformations and design space architectures for low-power embedded systems. In *Proceedings of the 2004 ACM symposium on Applied computing*, pages 891–896. ACM, 2004.

[C4] Giovanni Agosta, Stefano Crespi Reghizzi, Gerlando Falauto, and Martino Sykora. JIST: Just-In-Time scheduling translation for parallel processors. In *Third International Workshop on Parallel and Distributed Computing, 2004. Third International Symposium on/Algorithms, Models and Tools for Parallel Computing on Heterogeneous Networks, 2004.*, pages 122–132. IEEE, 2004.

[C5] Giovanni Agosta, Francesco Bruschi, Marco Santambrogio, and Donatella Sciuto. A data oriented approach to the design of reconfigurable stream decoders. In *3rd Workshop on Embedded Systems for Real-Time Multimedia, 2005.*, pages 107–112. IEEE, 2005.

[C6] Giovanni Agosta, Francesco Bruschi, and Donatella Sciuto. Aspect orientation in system level design. In *Proc. of Forum on Specification & Design Languages*, pages 397–400, 2005.

[C7] G Agosta, S Crespi Reghizzi, P Palumbo, and M Sykora. Selective compilation via fast code analysis and bytecode tracing. In *Proceedings of the 2006 ACM symposium on Applied computing*, pages 906–911. ACM, 2006.

[C8] Giovanni Agosta, Stefano Crespi Reghizzi, Dario Domizioli, and Martino Sykora. Global instruction scheduling in dynamic compilation for embedded systems. In *Proceedings of the 4th international workshop on Java technologies for real-time and embedded systems*, volume 177 of *ACM International Conference Proceeding Series*, pages 196–201. ACM, 2006.

[C9] Giovanni Agosta, Stefano Crespi Reghizzi, and Gabriele Svelto. Jelatine: a virtual machine for small embedded systems. In *Proceedings of the 4th international workshop on Java technologies for real-time and embedded systems*, ACM International Conference Proceeding Series, pages 170–177. ACM, 2006.

[C10] Giovanni Agosta, Marco D Santambrogio, and Seda Ogrenci Memik. Adaptive metrics for system-level functional partitioning. In *FDL*, pages 153–155, 2006.

[C11] Giovanni Agosta, Luca Breveglieri, Gerardo Pelosi, and Israel Koren. Countermeasures against branch target buffer attacks. In *Proceedings of the Workshop on Fault Diagnosis and Tolerance in Cryptography, FDTC 2007*, pages 75–79. IEEE, 2007.

[C12] Giovanni Agosta, Luca Breveglieri, Gerardo Pelosi, and Martino Sykora. Programming highly parallel reconfigurable architectures for public-key cryptographic applications. In *Information Technology, 2007. ITNG'07. Fourth International Conference on*, pages 3–10. IEEE, 2007.

[C13] Giovanni Agosta, Francesco Bruschi, Gerardo Pelosi, and Donatella Sciuto. A unified approach to canonical form-based boolean matching. In *Proceedings of the 44th annual Design Automation Conference*, pages 841–846. ACM, 2007.

[C14] Giovanni Agosta, Francesco Bruschi, and Donatella Sciuto. An efficient cost-based canonical form for Boolean matching. In *Proceedings of the 17th ACM Great Lakes symposium on VLSI (GLSVLSI)*, pages 445–448. ACM, 2007.

[C15] Giovanni Agosta and Gerardo Pelosi. A domain specific language for cryptography. In *Proceedings of the Forum on specification and Design Languages (FDL)*, pages 159–164, 2007.

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[C17] Martino Sykora, Giovanni Agosta, and Cristina Silvano. Dynamic configuration of application-specific implicit instructions for embedded pipelined processors. In *Proceedings of the 2008 ACM symposium on Applied computing*, pages 1509–1516. ACM, 2008.

[C18] Giovanni Agosta, Alessandro Barenghi, Fabrizio De Santis, Andrea Di Biagio, and Gerardo Pelosi. Fast disk encryption through GPGPU acceleration. In *Parallel and Distributed Computing, Applications and Technologies, 2009 International Conference on*, pages 102–109. IEEE, 2009.

[C19] Simone Campanoni, Martino Sykora, Giovanni Agosta, and Stefano Crespi Reghizzi. Dynamic look ahead compilation: a technique to hide jit compilation latencies in multicore environment. In *Compiler Construction*, pages 220–235. Springer, 2009.

[C20] Andrea Di Biagio, Alessandro Barenghi, Giovanni Agosta, and Gerardo Pelosi. Design of a parallel AES for graphics hardware using the CUDA framework. In *Parallel & Distributed Processing, 2009. IPDPS 2009. IEEE International Symposium on*, pages 1–8. IEEE, 2009.

[C21] Michele Tartara, Simone Campanoni, Giovanni Agosta, and Stefano Crespi Reghizzi. Just-In-Time compilation on ARM processors. In *Proceedings of the 4th workshop on the Implementation, Compilation, Optimization of Object-Oriented Languages and Programming Systems (ICOOOLPS 2009)*, pages 70–73. ACM, 2009.

[C22] Giovanni Agosta, Alessandro Barenghi, Fabrizio De Santis, and Gerardo Pelosi. Record setting software implementation of DES using CUDA. In *Information Technology: New Generations (ITNG), 2010 Seventh International Conference on*, pages 748–755. IEEE, 2010.

[C23] Andrea Di Biagio and Giovanni Agosta. Improved programming of gpu architectures through automated data allocation and loop restructuring. In *Architecture of Computing Systems (ARCS), 2010 23rd International Conference on*, pages 1–8. VDE, 2010.

[C24] C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A. Di Biagio, E. Speziale, M. Tartara, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Leupers, H. Meyr, J. Ansari, P. Mahonen, and B. Vanthournout. 2PARMA: Parallel paradigms and run-time management techniques for many-core architectures. pages 494–499, 2010.

[C25] Michele Tartara, Simone Campanoni, Giovanni Agosta, and Stefano Crespi Reghizzi. Parallelism and Retargetability in the ILDJIT Dynamic Compiler. In *Architecture of Computing Systems (ARCS), 2010 23rd International Conference on*, pages 1–7. VDE, 2010.

[C26] Giovanni Agosta, Marco Bessi, Eugenio Capra, and Chiara Francalanci. Dynamic memoization for energy efficiency in financial applications. In *Green Computing Conference and Workshops (IGCC), 2011 International*, pages 1–8. IEEE, 2011.

[C27] Andrea Di Biagio, Ettore Speziale, and Giovanni Agosta. Exploiting thread-data affinity in openmp with data access patterns. *Euro-Par 2011 Parallel Processing*, 6852 LNCS(PART 1):230–241, 2011.

[C28] C Silvano, W Fornaciari, S Crespi Reghizzi, G Agosta, G Palermo, V Zaccaria, P Bellasi, F Castro, S Corbetta, E Speziale, et al. Parallel paradigms and run-time management techniques for many-core architectures: The 2PARMA approach. In *Industrial Informatics (INDIN), 2011 9th IEEE International Conference on*, pages 835–840. IEEE, 2011.

[C29] Cristina Silvano, William Fornaciari, S Crespi Reghizzi, Giovanni Agosta, Gianluca Palermo, Vittorio Zaccaria, Patrick Bellasi, Fabrizio Castro, Simone Corbetta, Ettore Speziale, et al. Parallel programming and run-time resource management framework for many-core platforms: The 2PARMA approach (Invited paper). In *Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), 2011 6th International Workshop on*, pages 1–7. IEEE, 2011.

[C30] Ettore Speziale, Andrea Di Biagio, and Giovanni Agosta. An optimized reduction design to minimize atomic operations in shared memory multiprocessors. In *Parallel and Distributed Processing Workshops and Phd Forum (IPDPSW), 2011 IEEE International Symposium on*, pages 1300–1309. IEEE, 2011.

[C31] Giovanni Agosta, Alessandro Barenghi, Antonio Parata, and Gerardo Pelosi. Automated security analysis of dynamic web applications through symbolic code execution. In *Proceedings of the 9th International Conference on Information Technology, ITNG 2012*, pages 189–194, 2012.

[C32] Giovanni Agosta, Alessandro Barenghi, and Gerardo Pelosi. A code morphing methodology to automate power analysis countermeasures. In *Proceedings of the 49th Annual Design Automation Conference*, pages 77–82. ACM, 2012.

[C33] Giovanni Agosta, Alessandro Barenghi, and Gerardo Pelosi. Exploiting bit-level parallelism in gpgpus: A case study on keeloq exhaustive key search attack. In *ARCS Workshops (ARCS), 2012*, pages 1–7. IEEE, 2012.

[C34] Giovanni Agosta, Alessandro Barenghi, and Gerardo Pelosi. High speed cipher cracking: the case of Keeloq on CUDA. In *Proceedings of the 3rd Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures (PARMA 2012)*, 2012.

[C35] G Ascheid, B Stabernack, W Fornaciari, JM Zins, G Agosta, C Silvano, F Castro, D Melpignano, T Kempf, H Hübert, et al. Parallel paradigms and run-time management techniques for many-core architectures. In *2012 Interconnection Network Architecture on On-Chip, Multi-Chip Workshop-INA-OCMC'12*, pages 39–42. ACM, 2012.

[C36] Giovanni Agosta, Alessandro Barenghi, Massimo Maggi, and Gerardo Pelosi. Compiler-based side channel vulnerability analysis and optimized countermeasures application. In *Design Automation Conference (DAC), 2013 50th ACM/EDAC/IEEE*, pages 1–6. IEEE, 2013.

[C37] Giovanni Agosta, Alessandro Barenghi, Gerardo Pelosi, and Michele Scandale. Enhancing passive side-channel attack resilience through schedulability analysis of data-dependency graphs. In *International Conference on Network and System Security*, volume 7873 LNCS, pages 692–698. Springer Berlin Heidelberg, 2013.

[C38] Giovanni Agosta, Alessandro Barenghi, and Gerardo Pelosi. Securing software cryptographic primitives for embedded systems against side channel attacks. In *Proceedings - International Carnahan Conference on Security Technology*, volume 2014-October, 2014.

[C39] Giovanni Agosta, Alessandro Barenghi, Gerardo Pelosi, and Michele Scandale. A Multiple Equivalent Execution Trace Approach to Secure Cryptographic Embedded Software. In *Proceedings of the The 51st Annual Design Automation Conference on Design Automation Conference*, pages 1–6. ACM, 2014.

[C40] Giovanni Agosta, Alessandro Barenghi, Gerardo Pelosi, and Michele Scandale. Differential fault analysis for block ciphers: an automated conservative analysis. In *Proceedings of the 7th International Conference on Security of Information and Networks*, volume 2014-September of *ACM International Conference Proceeding Series*, pages 137–144, 2014.

[C41] Giovanni Agosta, Gerardo Pelosi, and Ettore Speziale. On task assignment in data intensive scalable computing. In *Workshop on Job Scheduling Strategies for Parallel Processing*, volume 8429 LNCS of *Lecture notess in Computer Science*, pages 136–155. Springer Berlin Heidelberg, 2014.

[C42] Iyad Al Khatib, Gerardo Pelosi, Giovanni Agosta, and Heikki Terio. Security Integration in Medical Device Design: Extension of an Automated Bio-Medical Engineering Design Methodology. In *ITNG 2014 - Proceedings of the 11th International Conference on Information Technology: New Generations*, pages 137–142. IEEE, 2014.

[C43] Davide Gadioli, Simone Libutti, Giuseppe Massari, Edoardo Paone, Michele Scandale, Patrick Bellasi, Gianluca Palermo, Vittorio Zaccaria, Giovanni Agosta, William Fornaciari, et al. OpenCL Application Auto-tuning and Run-Time Resource Management for Multi-core Platforms. In *Proceedings - 2014 IEEE International Symposium on Parallel and Distributed Processing with Applications, ISPA 2014*, pages 127–133, 2014.

[C44] Giuseppe Massari, Edoardo Paone, Michele Scandale, Patrick Bellasi, Gianluca Palermo, Vittorio Zaccaria, Giovanni Agosta, William Fornaciari, and Cristina Silvano. Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures. In *International Symposium on Applied Reconfigurable Computing*, volume 8405 LNCS, pages 345–352. Springer International Publishing, 2014.

[C45] G. Agosta, L. Borghese, C. Brandolese, F. Clasadonte, W. Fornaciari, F. Garzotto, M. Gelsomini, M. Grotto, C. Fra, D. Noferi, and M. Valla. Playful supervised smart spaces (p3s)-a framework for designing, implementing and deploying multisensory play experiences for children with special needs. In *Proceedings - 18th Euromicro Conference on Digital System Design, DSD 2015*, pages 158–164, 2015.

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[C62] Anna Pupykina and Giovanni Agosta. Optimizing Memory Management in Deeply Heterogeneous HPC Accelerators. In *Proceedings of the International Conference on Parallel Processing Workshops*, pages 291–300, 2017.

[C63] Giovanni Agosta, William Fornaciari, Giuseppe Massari, Anna Pupykina, Federico Reghenzani, and Michele Zanella. Managing Heterogeneous Resources in HPC Systems. In *Proceedings of the 9th Workshop and 7th Workshop on Parallel Programming and RunTime Management Techniques for Manycore Architectures and Design Tools and Architectures for Multicore Embedded Computing Platforms*, pages 7–12. ACM, 2018.

[C64] Daniele Cattaneo, Antonio Di Bello, Stefano Cherubin, Federico Terraneo, and Giovanni Agosta. Embedded Operating System Optimization through Floating to Fixed Point Compiler Transformation. In *Proceedings of the 2018 Euromicro Conference on Digital Systems Design*, pages 172–176, 2018.

[C65] S. Cherubin, G. Agosta, I. Lasri, E. Rohou, and O. Sentieys. Implications of Reduced-Precision Computations in HPC: Performance, Energy and Error. In *Advances in Parallel Computing*, volume 32, pages 297–306, 2018.

[C66] Ricardo Nobre, Luís Reis, João Bispo, Tiago Carvalho, João MP Cardoso, Stefano Cherubin, and Giovanni Agosta. Aspect-driven mixed-precision tuning targeting gpus. In *Proceedings of the 9th Workshop and 7th Workshop on Parallel Programming and RunTime Management Techniques for Manycore Architectures and Design Tools and Architectures for Multicore Embedded Computing Platforms*, pages 26–31. ACM, 2018.

[C67] Giovanni Agosta, Emanuele Baldino, Francesco Casella, Stefano Cherubin, Alberto Leva, and Federico Terraneo. Towards a high-performance modelica compiler. In *Proceedings of the 13th International Modelica Conference, Regensburg, Germany, March 4–6, 2019*, number 157. Linköping University Electronic Press, 2019.

[C68] Marco Festa, Nicole Gervasoni, Stefano Cherubin, and Giovanni Agosta. Continuous program optimization via advanced dynamic compilation techniques. In *Proceedings of the 10th and 8th Workshop on Parallel Programming and Run-Time Management Techniques for Manycore Architectures and Design Tools and Architectures for Multicore Embedded Computing Platforms*, page 2. ACM, 2019.

[C69] Andrea Gussoni, Alessandro Di Federico, Pietro Fezzardi, and Giovanni Agosta. Performance, correctness, exceptions: Pick three. In *Proceedings of Workshop on Binary Analysis Research (BAR) 2019*, 2019.

[C70] Cristina Silvano, Giovanni Agosta, Andrea Bartolini, Andrea R Beccari, Luca Benini, Loïc Besnard, João Bispo, Radim Cmar, João MP Cardoso, Carlo Cavazzoni, et al. Supporting the scale-up of high performance application to pre-exascale systems: The antarex approach. In *2019 27th Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP)*, pages 116–123. IEEE, 2019.

Other Publications

I have also co-authored and/or edited a number of technical works, including technical reports to the European Commission, most of which are not reported for the sake of brevity. Herebelow I report a selection of the most relevant and recent invited papers, posters, editorials, and publications in technical magazines.

[O1] Simone Campanoni, Giovanni Agosta, and Stefano Crespi Reghizzi. A parallel dynamic compiler for CIL bytecode. *ACM Sigplan Notices*, 43(4):11–20, 2008.

[O2] G. Agosta and E. Capra. Green software: anche le applicazioni consumano energia. *Mondo Digitale*, 10(1):9–24, 2011.

[O3] G Agosta, A Barenghi, M Maggi, and G Pelosi. Extending the design space for secure embedded system design. In *Work-in-Progress session at the 2014 Design Automation Conference (DAC'14)*, 2014.

[O4] G Pelosi, G Agosta, and I Al Khatib. Automated methodology integrating security and privacy in the design process of medical devices. In *Work-in-Progress session at the 2014 Design Automation Conference (DAC'14)*, 2014.

[O5] M. Cecowski, G. Agosta, A. Oleksiak, M. Kierzynka, M.V.D. Berge, W. Christmann, S. Krupop, M. Porrmann, J. Hagemeyer, R. Griessl, M. Peykanu, L. Tigges, S. Rosinger, D. Schlitt, C. Pieper, C. Brandolese, W. Fornaciari, G. Pelosi, R. Plestenjak, J. Cinkelj, L. Cudennec, T. Goubier, J.-M. Philippe, U. Janssen, and C. Adeniyi-Jones. The M2DC Project: Modular Microserver DataCentre (Invited paper). In *Proceedings - 19th Euromicro Conference on Digital System Design, DSD 2016*, pages 68–74, 2016.

[O6] A. Agneessens, F. Buemi, S. Delucchi, M. Massa, G. Agosta, A. Barenghi, C. Brandolese, W. Fornaciari, G. Pelosi, E. Ferrari, D. Cassioli, L. Pomante, L. Napoletani, L. Bozzi, C. Tieri, and M. Mongelli. Safe cooperative CPS: A V2I traffic management scenario in the SafeCOP project (Invited paper). In *Proceedings - 2016 16th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, SAMOS 2016*, pages 320–327, 2017.

[O7] José Flich, Giovanni Agosta, Philipp Ampletzer, David Atienza Alonso, Carlo Brandolese, Etienne Cappe, Alessandro Cilardo, Leon Dragić, Alexandre Dray, Alen Duspara, , W. Fornaciari, G. Guillaume, Y. Hoornenborg, A. Iranfar, M. Kovać, S. Libutti, B. Maitre, J.M. Martínez, G. Massari, H. Mlinarić, E. Papastefanakis, T. Picornell, I. Piljić, A. Pupykina, F. Reghenzani, I. Staub, R. Tornero, M. Zapater, and D. Zoni. MANGO: Exploring Manycore Architectures for Next-GeneratiOn HPC Systems (Invited paper). In *Proceedings - 20th Euromicro Conference on Digital System Design, DSD 2017*, pages 478–485, 2017.

[O8] A. Oleksiak, M. Kierzynka, G. Agosta, C. Brandolese, W. Fornaciari, G. Pelosi, M. Vor Dem Berge, W. Christmann, S. Krupop, M. Cecowski, R. Plestenjak, J. Cinkelj, M. Porrmann, J. Hagemeyer, R. Griessl, M. Peykanu, L. Tigges, L. Cudennec, T. Goubier, J.-M. Philippe, S. Rosinger, D. Schlitt, C. Pieper, C. Adeniyi-Jones, U. Janssen, and L. Ceva. Data centres for IoT applications: The M2DC approach (Invited paper). In *Proceedings - 2016 16th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, SAMOS 2016*, pages 293–299, 2017.

[O9] Federico Reghenzani, Giuseppe Massari, Anna Pupykina, Giovanni Agosta, and William Fornaciari. Resource and memory management in MANGO heterogeneous system. HiPEAC Summer School Posters, 2017.

[O10] Cristina Silvano, Andrea Bartolini, Andrea Beccari, Candida Manelfi, Carlo Cavazzoni, Davide Gadioli, Erven Rohou, Gianluca Palermo, Giovanni Agosta, Jan Martinovič, et al. The ANTAREX Tool Flow for Monitoring and Autotuning Energy Efficient HPC Systems (Invited paper). In *SAMOS 2017-International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation*, 2017.

[O11] Cristina Silvano, Giovanni Agosta, Andrea Bartolini, Andrea R. Beccari, Luca Benini, Loic Besnard, Joao Bispo, Radim Cmar, Joao M. P. Cardoso, Carlo Cavazzoni, Stefano Cherubin, Davide Gadioli, Martin Golasowski, Imane Lasri, Jan Martinovic, Gianluca Palermo, Pedro Pinto, Erven Rohou, Nico Sanna, Katerina Slaninova, and Emanuele Vitali. ANTAREX: A DSL-based Approach to Adaptively Optimizing and Enforcing Extra-Functional Properties in High Performance Computing. In *Proceedings of the 2018 Euromicro Conference on Digital Systems Design*, pages 600–607, 2018.

[O12] Giovanni Agosta, Carlo Brandolese, William Fornaciari, Nicholas Mainardi, Gerardo Pelosi, Federico Reghenzani, Michele Zanella, Gaetan Des Courchamps, Vincent Ducrot, Kevin Juilly, Sebastien Monot, and Luca Ceva. Accelerating automotive analytics: The m2dc appliance approach. In *Proceedings of the 2019 19th International Conference on Embedded Computing Systems: Architectures, Modeling and Simulation, SAMOS 2019 (to appear)*, 2019.

[O13] Giovanni Agosta, William Fornaciari, Alessandro Cilardo, José Flich Cardo, Carles Hernandez Luz, Michal Kulczewski, Giuseppe Massari, Rafael Tornero Gavilá, Marina Zapater Sancho, David Atienza Alonso, and Ramon Canal. Challenges in deeply heterogeneous high performance systems. In *Proceedings of the 2019 Euromicro Conference on Digital Systems Design*, 2019.

[O14] Daniele Cattaneo, Antonio Di Bello, Michele Chiari, Stefano Cherubin, and Giovanni Agosta. Fixed Point Exploitation via Compiler Analyses and Transformations. ACM International Conference on Computing Frontiers 2019 poster session, May 2019.

[O15] Giuseppe Massari, Anna Pupykina, Giovanni Agosta, and William Fornaciari. Predictive resource management for next-generation high-performance computing heterogeneous platforms. In *Proceedings of the 2019 19th International Conference on Embedded Computing Systems: Architectures, Modeling and Simulation, SAMOS 2019 (to appear)*, 2019.

[O16] Giovanni Agosta, Alessandro Barenghi, Israel Koren, and Gerardo Pelosi, editors. *CS2 '15: Proceedings of the Second Workshop on Cryptography and Security in Computing Systems*, New York, NY, USA, 2015. ACM.

[O17] Giovanni Agosta, Alessandro Barenghi, Israel Koren, and Gerardo Pelosi, editors. *CS2 '16: Proceedings of the Third Workshop on Cryptography and Security in Computing Systems*, New York, NY, USA, 2016. ACM.

[O18] Giovanni Agosta, Alessandro Barenghi, and Gerardo Pelosi, editors. *CS2 '17: Proceedings of the Fourth Workshop on Cryptography and Security in Computing Systems*, New York, NY, USA, 2017. ACM.

[O19] Giovanni Agosta, Cristina Silvano, João Cardoso, and Michael Huebner, editors. *PARMA-DITAM '15: Proceedings of the 6th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures*, New York, NY, USA, 2015. ACM.

[O20] Cristina Silvano, João Cardoso, Giovanni Agosta, and Michael Huebner, editors. *PARMA-DITAM '16: Proceedings of the 7th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and the 5th Workshop on Design Tools and Architectures For Multicore Embedded Computing Platforms*, New York, NY, USA, 2016. ACM.

Invited Talks

2015 G. Agosta. "The MANGO FET-HPC Project: An Overview", held at 18th IEEE Conference on Computational Science and Engineering, Special Session on FET-HPC and Exascale Recently EU-Funded Projects, Porto (Portugal), October 2015.

2010 G. Agosta, "Application Virtualization: The 2PARMA Approach", held at HiPEAC Virtualization Cluster Meeting, October 2010, Barcelona, Spain.

2010 G. Agosta, "The 2PARMA Compiler Toolchain", held at HiPEAC Compilation Cluster Meeting, October 2010, Barcelona, Spain.

Software

I have supervised and participated to the development of numerous software packages. I report here only the major packages for which I either had a primary design role, or coordinated a development team across multiple years.

2017-current MANGOLIBS, a parallel programming model for deeply heterogeneous architectures integrating resource management.
Role: scientific leadership, design and implementation of the first two versions [C63] (the current version is co-developed with Federico Reghenzani and Anna Pupykina).

2016-current LIBVERSIONINGCOMPILER, a library for easy dynamic code versioning and specialization.
Role: scientific leadership, design and implementation of the first version (superceded by the current version [J16], developed by Stefano Cherubin).

2012-current OPENCRUN, an implementation of the OpenCL programming model [C43].
Role: scientific leadership (design and development by Ettore Speziale, Michele Scandale, and Giulio Sichel).

CODE MORPHING ENGINE, a polymorphic engine for the generation of semantically equivalent code fragments employed in protecting the software implementation of cryptographic primitives against side channel attacks [C32].
Role: scientific co-leadership, design and implementation (co-leadership by Gerardo Pelosi).

2008-2010 JIST, a just-in-time compiler for VLIW architectures featuring efficient instruction scheduling [C4, J1].
Role: scientific leadership, design (developed primarily by Martino Sykora and Gerlando Falauto).

Declarations stated in this curriculum are to be taken as given according to the articles artt. 46 e 47 of D.P.R. 445/2000.

I authorize the treatment of personal data according to the privacy regulations of D.Lgs. n. 196/2003, ”Codice in materia di protezione dei dati personali”, and subsequent modifications.

Le dichiarazioni rese nel presente curriculum sono da ritenersi rilasciate ai sensi degli artt. 46 e 47 del D.P.R. 445/2000.

Autorizzo il trattamento dei dati personali ai sensi del D.Lgs. n. 196/2003, ”Codice in materia di protezione dei dati personali”, e seguenti modifiche.

Milano, November 7, 2019